Image

Docket No.: 57454-178 PATENT 2822

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Shoichiro NAKAZAWA, et al.	:	Confirmation Number: 7532
Serial No.: 09/915,567	:	Group Art Unit: 2822
Filed: July 27, 2001	:	Examiner: I.M. Soward

For: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE (AS AMENDED)

TRANSMITTAL OF APPEAL BRIEF

Mail Stop
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed December 15, 2003. Please charge the Appeal Brief fee of to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Arthur J. Steiner
Registration No. 26,106

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Date: February 4, 2004

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The real party in interest is Renesas Corp.

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Appellants are unaware of any related Appeal or Interference.

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Claims 1 through 11 are pending in this application, of which claims 1 through 6 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R. §1.142(b). Claims 7 through 11

have been finally rejected. It is from the final rejection of claims 7 through 11 that this Appeal is taken.

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No Amendment has been filed subsequent to the issuance of the Final Office Action dated July 14, 2003. However, a Request for Reconsideration was filed on October 14, 2003. According to the Advisory Action of November 19, 2003, the Request for Reconsideration was considered by the Examiner, but not found persuasive.

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The present invention stems from the recognition that a void formed in the gap between closely spaced transfer gates can lead to short circuiting in between neighboring polypads 104a and 104b (Fig. 17), because the polysilicon employed for depositing the polypads enters the void, thereby reducing product yield (paragraph bridging pages 1 and 2 of the written description of the specification). Appellants address and solved that problem which they recognized attendant upon conventional practices by depositing a short-circuit preventing insulating film, such as a nitride film 5, on the surfaces of the sidewalls of insulating layer 8 and transfer gates 3 (paragraph bridging pages 8 and 9 of the written description of the specification; Figs. 1-3).

VI. ISSUES

A. The Rejection

Claims 7 through 11 stand finally rejected under 35 U.S.C. 103 for obviousness predicated upon the acknowledged prior art (Figs. 15-17) in view of Saitoo et al.

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Whether claims 7 through 11 are unpatentable under 35 U.S.C. 103 for obviousness predicated upon the acknowledged prior art (Figs. 15 through 17) in view of Saitoo et al.

VII. GROUPING OF CLAIMS

The appealed claims stand or fall together as a group with independent claim 7.

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There is no admission

The present invention stems from the recognition of a short circuiting problem attendant upon conventional practices when gap filling between closely spaced transfer gates leaving a void subsequently filled with conductive material at the time of depositing polypads. Thus the invention encompassed by independent claim 7 is directed to a semiconductor device with a short-circuit preventing film which prevents short circuiting between plug interconnections. Appellants have clarified the record by attempting to disabuse the Examiner of the notion that Appellants admitted that the problem addressed and solved by the claimed invention was known. Rather, the problem addressed and solved by the claimed invention was appreciated by Appellants.

Notwithstanding, Appellants disavowal of any admission, the Examiner's rejection appears to **assume** that Appellants admitted recognition of the short-circuit problem addressed and solved by the claimed invention. Given that recognition, the Examiner simplifies the issue on Appeal by concluding that one having ordinary skill in the art would have employed a short-circuit preventing film in a situation where short-circuiting is appreciated. But absent that admission, the Examiner's rejection

falls for lack of the requisite fact-based motivation. *In re Lee, 237 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).*

The pivotal issue.

The Examiner begins by admitting that the acknowledged prior art does not show a short-circuit preventing insulating film. The Examiner finds a short-circuit preventing insulating film in Saitoo et al., notably films 28 appearing in Figs. 18 and 19. Absent any admission that the short-circuiting problem attendant upon conventional practices was recognized, the issue which arises is: **What is the factual basis to support the Examiner's assertion that the problem disclosed by Saitoo et al. "... would have been recognized in the pertinent art of Admitted Prior Art Figures 15-17" (sentence bridging pages 2 and 3 of the Final Office Action dated July 14, 2003)?** Simply put, there is no factual basis to support the Examiner's position. Appellants would rely upon the decision in *Teleflex Inc. v. Ficosa North America Corp., 299 F.3d 1313, 63 USPQ2d 1374, 1387 (Fed. Cir. 2002)*, wherein the court held:

> The showing of a motivation to combine must be clear and particular, and it must be supported actual evidence.

In the present case, the Examiner provided no facts to support the asserted motivation. Indeed, in the July 7, 2003 Final Office Action and in the November 19, 2003 Advisory Action, the Examiner dances around the problem recognition element, asserting it would have been recognized. In other words, the Examiner assumes into existence art recognition without providing facts. This flunks the judicial test for motivation. *Teleflex Inc. v. Ficosa North America Corp., supra.; In re Lee, supra.*

The Examiner's position

After being challenged as to the motivational element expressed in the Final Office Action, the Examiner responded in the Advisory Action by asserting:

> In this case, the semiconductor device of Saitoo et al. disclose several benefits of utilizing a short-circuit preventing insulating film in columns 23-24, lines 48-68 and 1-68, respectively; benefits that can be utilized in the semiconductor device of Admitted Prior Art Figures 15-17 (continuation sheet of the Advisory Action).

Appellants have reviewed the passages mentioned by the Examiner, but find no relationship between such passages and the **particular short-circuiting problem** addressed and solved by the claimed invention attendant upon forming interconnects due to conductive material flowing into a void formed between closely spaced apart transfer gates (paragraph bridging 1 and 2 of the written description of the specification). Saying that one having ordinary skill in the art would somehow have divined a reason to correct an unappreciated problem attendant upon conventional practices by referring to two passages in Saitoo et al. directed to an unrelated problem is one thing; providing the requisite fact-based reasoning is quite another. *In re Lee, supra.*

Not only has the Examiner failed to establish the requisite fact-based realistic motivational element, but there are significant differences between the disclosure of Saitoo et al. and the particular problem addressed and solved by the claimed invention which undermines the Examiner's generalized motivational approach to the obviousness conclusion. Specifically, the entire structure of and purpose for film 28 employed by Saitoo et al. are completely **different** from any problem which the Examiner asserts, but does not back up with facts because the Examiner cannot, would have been recognized in the acknowledged prior art. The film 28 employed by Saitoo et al. comprises **stacked flat layers**, which would **not** appear to be particular useful in preventing the short-circuiting problem addressed

and solved by the claimed invention attendant upon Figs. 15-17. In accordance with the claimed invention, a short-circuit preventing insulating film 5 has a cylindrical shape or a pipe-like shape.

Moreover, the structure surrounding film 28 of Saitoo et al. is **predetermined** and fabricated without variation under defined processing conditions. Accordingly, film 28 is **always** effective in functioning as an insulator. There is no uncertainty. There is no unpredictability.

However, the present invention addresses a problem wherein it is indefinite as to where void 9 may or may not form, and whether or not the conducting material or polysilicon 114 causes short-circuiting. Thus, the present invention is designed to solve a problem generated by two indefinite factors. The film 5 employed by the present invention **solves that problem when both of these undesirable conditions occur**. Not so in Saitoo et al. where everything is predictable.

Furthermore, film 5 of the present invention is meaningless if void 9 is not generated. But when void 9 is generated, it effectively functions as an insulator to prevent short-circuiting. On the other hand, in Saitoo et al., film 28 is **always** effective in functioning as an insulator because everything is predetermined.

The above argued differences in the structure and objective between Saitoo et al. and the present invention exacerbate the lack of fact-based motivation because of the different purpose for which the short-circuiting film of Saitoo is designed. As previously pointed out, film 28 employed by Saitoo et al. is built into a predetermined, predesigned structure wherein it is **always** effective. However, the present invention addresses and solves an entirely different problem which, again, has not been factually established as recognized in the art. That problem, which Appellants discovered, involves **uncertainty** as to where void 9 may or may not form and whether polysilicon 114 may or may not cause short-circuiting.

The Examiner has **not** provided a **fact-based explanation why** one having ordinary skill in the art would have resorted to the predictable, predesigned structure of Saitoo et al. to address **unrecognized** problems of uncertainty in Figs. 15 through 17, even **if** one having ordinary skill in the art would have been presumed to be aware of such problems- and Appellants maintain the Examiner has not provided a factual basis to establish art-recognition of such a problem in the acknowledged prior art (Figs. 15 through 17). *Teleflex Inc. v. Ficosa North America Corp., supra.* Because of the unpredictability of the short-circuiting problem illustrated in Figs. 15-17, one skilled in the art would **not** have **assumed** the existence of the same unappreciated problem as in Saitoo et al.

Conclusion

Based upon the foregoing, Appellants submit the Examiner did not establish a prima facie basis to deny patentability to the claimed invention for lack of the requisite factual basis and want of the requisite realistic motivation. Moreover, upon giving due consideration to the **problem** discovered by Appellants, the conclusion appears inescapable that one having ordinary skill in the art would **not** have found the claimed invention **as a whole** obvious within the meaning of 35 U.S.C. §103. *In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).*

Appellants, therefore, submit that the imposed rejection of claims 7 through 11 under 35 U.S.C. §103 for obviousness predicated upon the acknowledged prior art (Figs. 15 through 17) in view of Saitoo et al. is not factually or legally viable.

IX. PRAYER FOR RELIEF

Based upon the arguments submitted supra., Appellants submit that the Examiner's rejection under 35 U.S.C. 103 is not factually or legally viable. Appellants, therefore, solicit The Honorable Board to reverse the Examiner's rejection of the appealed claims under 35 U.S.C. 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

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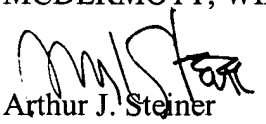

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X. APPENDIX

1. A method of manufacturing a semiconductor device, comprising:

a close wiring layer forming step of forming a plurality of wiring layers in parallel and close to each other with a gap between neighboring wiring layers on a base layer which is either a semiconductor layer or a conducting layer;

an insulating layer depositing step of depositing an insulating layer covering said wiring layer so as to bury said gap;

a contact hole opening step of opening two or more contact holes at an interval in said insulating layer along the longitudinal direction of said gap in a plan view;

a short-circuit preventing insulating film depositing step of depositing a short-circuit preventing insulating film in said contact hole;

a short-circuit preventing film removing step of removing at least said short-circuit preventing insulating film on the bottom of said contact hole to expose said base layer; and

a plug interconnection forming step of forming a plug interconnection in contact with said base layer by using a conductive material so as to bury said contact hole.

2. The method of manufacturing a semiconductor device according to claim 1, wherein said close wiring layer forming step includes a covering insulating film forming step of forming a covering insulating film covering each of wiring layers formed on said base layer and the base layer in said gap.

3. The method of manufacturing a semiconductor device according to claim 2, wherein in said contact hole opening step, a contact hole is opened so as to reach the covering insulating film

which covers said base layer of the bottom of said gap formed in said covering insulating film forming step.

4. The method of manufacturing a semiconductor device according to claim 2, wherein said contact hole opening step includes a covering insulating film removing step of removing the covering insulating film covering said base layer of the bottom of said gap to expose said base layer.

5. The method of manufacturing a semiconductor device according to claim 1, wherein in said short-circuit preventing insulating film depositing step, at least one of a silicon nitride film and a silicon oxide film is deposited by CVD.

6. The method of manufacturing a semiconductor device according to claim 1, wherein said plurality of wiring layers are a transfer gate as a word line, and said plug interconnection is a polypad which connects said base layer and a bit line.

7. A semiconductor device comprising:

a plurality of wiring layers disposed in parallel so as to be close to each other with a gap on a base layer which is either a semiconductor layer or a conductive layer;

an insulating layer disposed so as to bury said gap and cover said wiring layers; and

two or more plug interconnections made of a conductive material reaching said base layer, which are disposed at an interval in a part of said insulating layer along the longitudinal direction of said gap in a plan view,

wherein a short-circuit preventing insulating film different from said insulating layer is provided between said plug interconnection and said insulating layer.

8. The semiconductor device according to claim 7, wherein said short-circuit preventing insulating film enters a void occurring in a portion which buries said gap in said insulating layer.

9. The semiconductor device according to claim 7, wherein said short-circuit preventing insulating film is at least one of a silicon nitride film and a silicon oxide film.

10. The semiconductor device according to claim 7, wherein said conductive material is polysilicon containing an impurity.

11. The semiconductor device according to claim 7, wherein said plurality of wiring layers are a transfer gate serving as a word line, and said plug interconnection is a polypad connecting said base layer and a bit line.

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Conclusion

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Appellants, therefore, submit that the imposed rejection of claims 7 through 11 under 35 U.S.C. §103 for obviousness predicated upon the acknowledged prior art (Figs. 15 through 17) in view of Saitoo et al. is not factually or legally viable.

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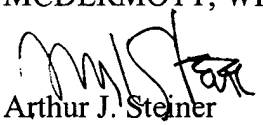

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X. APPENDIX

1. A method of manufacturing a semiconductor device, comprising:

a close wiring layer forming step of forming a plurality of wiring layers in parallel and close to each other with a gap between neighboring wiring layers on a base layer which is either a semiconductor layer or a conducting layer;

an insulating layer depositing step of depositing an insulating layer covering said wiring layer so as to bury said gap;

a contact hole opening step of opening two or more contact holes at an interval in said insulating layer along the longitudinal direction of said gap in a plan view;

a short-circuit preventing insulating film depositing step of depositing a short-circuit preventing insulating film in said contact hole;

a short-circuit preventing film removing step of removing at least said short-circuit preventing insulating film on the bottom of said contact hole to expose said base layer; and

a plug interconnection forming step of forming a plug interconnection in contact with said base layer by using a conductive material so as to bury said contact hole.

2. The method of manufacturing a semiconductor device according to claim 1, wherein said close wiring layer forming step includes a covering insulating film forming step of forming a covering insulating film covering each of wiring layers formed on said base layer and the base layer in said gap.

3. The method of manufacturing a semiconductor device according to claim 2, wherein in said contact hole opening step, a contact hole is opened so as to reach the covering insulating film

which covers said base layer of the bottom of said gap formed in said covering insulating film forming step.

4. The method of manufacturing a semiconductor device according to claim 2, wherein said contact hole opening step includes a covering insulating film removing step of removing the covering insulating film covering said base layer of the bottom of said gap to expose said base layer.

5. The method of manufacturing a semiconductor device according to claim 1, wherein in said short-circuit preventing insulating film depositing step, at least one of a silicon nitride film and a silicon oxide film is deposited by CVD.

6. The method of manufacturing a semiconductor device according to claim 1, wherein said plurality of wiring layers are a transfer gate as a word line, and said plug interconnection is a polypad which connects said base layer and a bit line.

7. A semiconductor device comprising:

a plurality of wiring layers disposed in parallel so as to be close to each other with a gap on a base layer which is either a semiconductor layer or a conductive layer;

an insulating layer disposed so as to bury said gap and cover said wiring layers; and

two or more plug interconnections made of a conductive material reaching said base layer, which are disposed at an interval in a part of said insulating layer along the longitudinal direction of said gap in a plan view,

wherein a short-circuit preventing insulating film different from said insulating layer is provided between said plug interconnection and said insulating layer.

8. The semiconductor device according to claim 7, wherein said short-circuit preventing insulating film enters a void occurring in a portion which buries said gap in said insulating layer.

9. The semiconductor device according to claim 7, wherein said short-circuit preventing insulating film is at least one of a silicon nitride film and a silicon oxide film.

10. The semiconductor device according to claim 7, wherein said conductive material is polysilicon containing an impurity.

11. The semiconductor device according to claim 7, wherein said plurality of wiring layers are a transfer gate serving as a word line, and said plug interconnection is a polypad connecting said base layer and a bit line.